CLAIMS

What is claimed is:

1. A system comprising:

a host/data controller; and

a memory system comprising a plurality of memory cartridges operably coupled to the host/data controller, each memory cartridge comprising an operation indicator configured to indicate the operational status of the corresponding memory cartridge.

2. The system, as set forth in claim 1, wherein the memory system comprises a redundant memory system.

3. The system, as set forth in claim 2, wherein the memory system comprises five memory cartridges.

4. The system, as set forth in claim 3, wherein the operation indicator comprises a bit having a first state and a second state, the first state indicating that the memory cartridge is operational and the second state indicating that the memory cartridge is not operational.

5. The system, as set forth in claim 4, wherein the memory system is configured to operate in a redundant mode when each of the bits is in the first state.

6. The system, as set forth in claim 5, wherein at least one of the host/data controller and the plurality of memory cartridges comprise error detection components.

7. The system, as set forth in claim 6, wherein the host/data controller is configured to generate a low priority interrupt signal in response to error detection by the error detection components if each of the operation bits is in the first state.

8. The system, as set forth in claim 6, wherein the host/data controller is configured to generate a low priority interrupt signal in response to multi-bit error detection by the error detection components if each of the operation bits is in the first state.

9. The system, as set forth in claim 6, wherein the host/data controller is configured to generate a high priority interrupt signal in response to multi-bit error detection if at least one of the operation bits is in the second state.

10. The system, as set forth in claim 1, wherein each of the plurality of memory cartridges comprises a plurality of memory devices.

11. A method of generating interrupts in a redundant memory, comprising the acts of:

detecting an error in a memory system;

determining the operational status of the memory system; and

initiating a system interrupt signal, the type of system interrupt signal being dependent on the operational status of the memory system.

12. The method, as set forth in claim 11, wherein the act of detecting an error comprises the act of detecting a multi-bit error.

13. The method, as set forth in claim 11, wherein the act of determining the operational status comprises the act of determining whether the system is operating in one of a redundant mode and a non-redundant mode.

14. The method, as set forth in claim 13, wherein the act of determining the operational status comprises reading a plurality of operation bits, each of the operation bits indicating the operational status of a corresponding segment of the memory, the operational status comprising one of an operational state and a non-operational state.

15. The method, as set forth in claim 14, wherein the act of determining the operational status comprises reading five operation bits.

16. The method, as set forth in claim 15, wherein the act of initiating a system interrupt comprises the act of initiating a low priority system interrupt if each of the five operation bits is in the operational state.

17. The method, as set forth in claim 15, wherein the act of initiating a system interrupt comprises the act of initiating a high priority system interrupt if any of the five operation bits is in the non-operational state.

18. A memory cartridge comprising:

a plurality of memory modules; and

a memory controller operably coupled to each of the plurality of memory modules and comprising a programmable masking register configured to store an error identification corresponding to one of the plurality of memory modules in which an error has been detected.

19. The memory cartridge, as set forth in claim 18, wherein each of the plurality of memory modules comprises a dual inline memory module (DIMM).

20. The memory cartridge, as set forth in claim 19, wherein each of the dual inline memory modules comprises a plurality of synchronous dynamic random access memory (SDRAM) devices.

21. The memory cartridge, as set forth in claim 18, wherein the programmable masking register is configured to store a chip select corresponding to one of the plurality of memory modules in which an error has been detected.

22. The memory cartridge, as set forth in claim 18, comprising compare logic configured to compare the error identification stored in the programmable masking register to any error identification corresponding to any subsequent errors detected in one of the plurality of memory modules.

23. The memory cartridge, as set forth in claim 22, comprising configuration logic configured to block the generation of an interrupt signal from the memory controller if the error identification stored in the programmable masking register matches the error identification corresponding to any subsequent errors.

24. A method of masking the error generation in a memory module comprising the acts of:

detecting a faulty memory module;

storing a unique memory module identification corresponding to the faulty memory module in a masking register;

detecting errors in a plurality of memory modules each memory module comprising a corresponding unique memory module identification;

comparing each of the memory module identifications in which an error is detected with the memory module identification corresponding to the faulty memory module; and

blocking the generation of errors to a host/data controller if the memory module identification corresponding to the memory module in which an error is detected is the same as the memory module identification corresponding to the faulty memory module.

25. The method of masking the error generation in a memory module, as set forth in claim 24, wherein the act of detecting a faulty memory module comprises the act of detecting the faulty memory module in a memory cartridge.

26. The method of masking the error generation in a memory module, as set forth in claim 25, wherein the act of detecting errors in a plurality of memory modules comprises the act of detecting errors in a plurality of memory modules in the memory cartridge.

27. The method of masking the error generation in a memory module, as set forth in claim 24, wherein the act of detecting a faulty memory module comprises the act of detecting the faulty dual inline memory module (DIMM).

28. The method of masking the error generation in a memory module, as set forth in claim 24, wherein the act of storing a unique memory module identification comprises the act of storing a chip select corresponding to the faulty memory module.

29. The method of masking the error generation in a memory module, as set forth in claim 26, wherein the act of storing comprises storing a unique memory module identification corresponding to the faulty memory module in a masking register, wherein the masking register is on the memory cartridge.

30. A computer system comprising:

a host/data controller;

a plurality of memory cartridges operably coupled to the host/data controller, each of the plurality of memory cartridges comprising a memory controller;

a command bus operably coupled between the host/data controller and the plurality of memory controllers and configured to transmit commands from the host/data controller to the plurality of memory controllers; and

error detection logic located on the command bus and configured to detect errors on the command bus.

31. The computer system, as set forth in claim 30, wherein the plurality of memory cartridges form a redundant memory array.

32. The computer system, as set forth in claim 30, wherein each of the plurality of memory cartridges comprises a plurality of memory modules, each of the plurality of memory modules comprising a plurality of memory devices.

33. The computer system, as set forth in claim 32, wherein each of the plurality of memory cartridges comprises a plurality of dual inline memory modules (DIMM), each of the plurality of memory modules comprising a plurality of synchronous dynamic random access memory (SDRAM) devices.

34. The computer system, as set forth in claim 30, comprising a command bus interface coupled between the plurality of memory cartridges and the error detection logic, the command bus interface configured to facilitate the exchange of data and commands between the host/data controller and the plurality of memory cartridges.

35. The computer system, as set forth in claim 34, comprising decode logic coupled between the command bus interface and the plurality of memory cartridges and configured to translate a system address into a memory address and a memory address into a system address for associated read and write commands between the host/data controller and the plurality of memory controllers.

36. The computer system, as set forth in claim 30, wherein the error detection logic comprises an ECC algorithm.

37. The computer system, as set forth in claim 30, wherein the error detection logic is configured to correct single bit errors on the command bus.

38. The computer system, as set forth in claim 30, wherein the error detection logic is configured to detect multi-bit errors on the command bus and further configured to transmit an unrecoverable command error message to the host/data controller when an unrecoverable multi-bit error is detected on the command bus.

39. A method of exchanging information in a redundant memory system, comprising the acts of:

detecting errors on a command bus, the errors comprising one of a single bit error and a multi-bit error;

correcting any single bit errors detected on the command bus; and

generating an error message if a multi-bit error is detected on the command bus.

40. The method of exchanging information, as set forth in claim 39, wherein the act of correcting comprises the act of correcting any single bit errors detected on the command bus using an ECC algorithm.

41. The method of exchanging information, as set forth in claim 39, wherein the act of detecting errors, comprises the act of detecting errors on a command bus, the command bus operably coupled between a host/data controller and a plurality of memory cartridges configured to form a redundant memory system.

42. The method of exchanging information, as set forth in claim 41, wherein the act of generating comprises the act of generating an error message from error detection logic located on the command bus to the host/data controller.

43. The method of exchanging information, as set forth in claim 42, comprising the act of powering down the memory cartridge in which the multi-bit error is detected in response to the error message generated from the error detection logic.

44. A memory cartridge comprising:

a plurality of memory modules, each of the plurality of memory modules comprising a reserved segment of non-volatile memory configured to store information unique to the corresponding memory module; and

a memory controller configured to detect errors in each of the plurality of memory modules and configured to facilitate storage of information correlative to the errors detected in the plurality of memory modules in the respective reserved segment of non-volatile memory.

45. The memory cartridge, as set forth in claim 44, wherein the plurality of memory modules comprises a plurality of dual inline memory modules (DIMMs).

46. The memory cartridge, as set forth in claim 44, wherein each of the plurality of reserved segments of non-volatile memory is configured to store identification information corresponding to the respective memory module.

47. The memory cartridge, as set forth in claim 44, wherein each of the plurality of reserved segments of non-volatile memory comprises 128 bytes of memory.

48. The memory cartridge, as set forth in claim 44, wherein the memory controller comprises ECC logic to detect errors in each of the plurality of memory modules.

49. The memory cartridge, as set forth in claim 44, wherein the memory controller is configured to receive error information from a host/data controller, the error information correlative to errors detected in the plurality of memory modules, and wherein the memory controller is further configured to facilitate storage of the error information from the host/data controller in the respective reserved segment of non-volatile memory.

50. A method of storing information on a memory module, comprising the acts of:

accessing an IIC interface on the memory module, the IIC interface comprising a non-volatile memory segment; and

storing identification information correlative to the memory module in the IIC interface.

51. The method of storing information on a memory module, as set forth in claim 50, wherein the act of accessing comprises the act of accessing an IIC interface on a dual inline memory module.

52. The method of storing information on a memory module, as set forth in claim 50, wherein the act of storing comprises the act of storing a unique module identification number correlative to the memory module.

53. A method of storing error detection information on a memory module comprising the acts of:

detecting an error on the memory module; and

storing information correlative to the error in a reserved segment of the memory module, the reserved segment comprising non-volatile memory.

54. The method of storing error detection information, as set forth in claim 53, wherein the act of detecting comprises the act of detecting an error on the memory module using an ECC algorithm.

55. The method of storing error detection information, as set forth in claim 53, wherein the act of storing comprises the act of storing an error type correlative to the type of error.

56. The method of storing error detection information, as set forth in claim 53, wherein the act of storing comprises the act of storing an address correlative to the address in which the error is detected.

57. A computer system comprising:

a memory cartridge comprising a plurality of memory modules, the memory cartridge configured to be hot-pluggable and wherein each of the memory modules

comprises a plurality of addresses corresponding to storage locations in the memory modules;

a host/data controller coupled to the memory cartridge and configured to facilitate a hot plug operation;

an address register configured to incrementally track the hot plug operation through the corresponding plurality of addresses; and

an indication device configured to provide a user with optical indication of progress of the hot plug operation.

58. The computer system, as set forth in claim 57, wherein the plurality of memory modules comprises a plurality of dual inline memory modules (DIMMs).

59. The computer system, as set forth in claim 57, wherein the host/data controller comprises software configured to monitor the address register and to provide an output signal corresponding to the a percentage of address registers which have completed the hot plug operations.

60. The computer system, as set forth in claim 59, wherein the indication device is configured to receive the output signal from the host/data controller.

61. The computer system, as set forth in claim 60, wherein the indication device is configured to provide an optical indication correlative to the output signal.

62. The computer system, as set forth in claim 57, wherein the hot plug operation comprises an initialization procedure to initialize the memory cartridge.

63. The computer system, as set forth in claim 57, wherein the hot plug operation comprises a rebuilding procedure to write data to the memory cartridge.

64. The computer system, as set forth in claim 57, wherein the hot plug operation comprises a verifying procedure to validate data written to the memory cartridge.

65. The computer system, as set forth in claim 57, wherein the address register comprises an entry for each address in the memory cartridge.

66. The computer system, as set forth in claim 57, wherein the indicator device comprises a plurality of light emitting diodes (LEDs).

67. The computer system, as set forth in claim 66, wherein the indication device comprises four light emitting diodes (LEDs).

68. A method of providing a user with progress status during a memory cartridge replacement procedure in a redundant memory system comprising the acts of:

inserting a memory cartridge into a system;

initiating a hot-plug procedure;

tracking the incremental progress of the hot-plug procedure; and

providing an optical indication correlative to the incremental progress.

69. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 68, wherein the act of inserting comprises the act of manually inserting the memory cartridge into the system.

70. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 68, wherein the act of initiating comprises the act of initiating an initialization procedure to initialize the memory cartridge.

71. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 68, wherein the act of initiating comprises the act of initiating a rebuilding procedure to write reconstructed data to the memory cartridge.

72. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 71, wherein the act of initiating comprises the act of initiating a verification procedure to verify the validity of reconstructed data written to the memory cartridge.

73. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 68, wherein the act of tracking comprises the act of monitoring a configuration register.

74. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 68, wherein the act of providing comprises the act of providing a user with an optical indication correlative to the incremental progress.

75. The method of providing a user with progress status during a memory cartridge replacement procedure, as set forth in claim 74, wherein the act of providing comprises the act of illuminating one or more light emitting diodes (LEDs) correlative to the incremental progress.

76. A method of manufacturing a redundant memory system comprising the acts of:

providing one or more hot-pluggable redundant memory segments; and

providing an indicator device to indicate the incremental progress of a hot-plug procedure.

77. The method of manufacturing a redundant memory system, as set forth in claim 76, wherein the act of providing an indicator device comprises the act of providing an optical indicator device.

78. The method of manufacturing a redundant memory system, as set forth in claim 77, wherein the act of providing an optical indicator device comprises the act of providing one or more light emitting diodes (LEDs).

79. A system comprising:

a redundant memory system comprising a plurality of memory cartridges, wherein each memory cartridge comprises a corresponding cartridge indicator; and

a terminal operably coupled to the redundant memory system and located remotely with respect to the redundant memory system, wherein the terminal is configured to initiate a cartridge signal to activate the cartridge indicator.

80. The system, as set forth in claim 79, wherein each of the plurality of cartridge indicators comprises a light emitting diode (LED).

81. The system, as set forth in claim 80, wherein the terminal is configured to initiate a cartridge signal to illuminate the light emitting diode (LED).

82. The system, as set forth in claim 79, wherein the terminal is configured to initiate the cartridge signal to activate the cartridge indicator in response to a user-selected command entered at the terminal.

83. The system, as set forth in claim 79, wherein each of the plurality of memory cartridges comprises a plurality of memory modules and a module indicator corresponding to each of the memory modules; and wherein the terminal is configured to initiate a module signal to activate the corresponding module indicator.

84. The system, as set forth in claim 83, wherein each of the plurality of module indicators comprises a light emitting diode (LED).

85. The system, as set forth in claim 84, wherein the terminal is configured to initiate a module signal to illuminate the light emitting diode (LED).

86. The system, as set forth in claim 83, wherein the terminal is configured to initiate the module signal to activate the module indicator in response to a user-selected command entered at the terminal.

87. A method of identifying a memory portion in a redundant memory system comprising the acts of:

initiating a command from a terminal, the terminal being located remotely with respect to the system; and

activating an illumination device on the memory portion in response to the command from the terminal.

88. The method of identifying a memory portion in a redundant memory system, as set forth in claim 87, wherein the act of initiating comprises the act of initiating the command by a user.

89. The method of identifying a memory portion in a redundant memory system, as set forth in claim 87, wherein the act of activating comprises the act of activating a light emitting diode (LED) in response to the command from the terminal.

90. The method of identifying a memory portion in a redundant memory system, as set forth in claim 87, wherein the memory portion comprises a memory cartridge.

91. The method of identifying a memory portion in a redundant memory system, as set forth in claim 87, wherein the memory portion comprises a memory module.